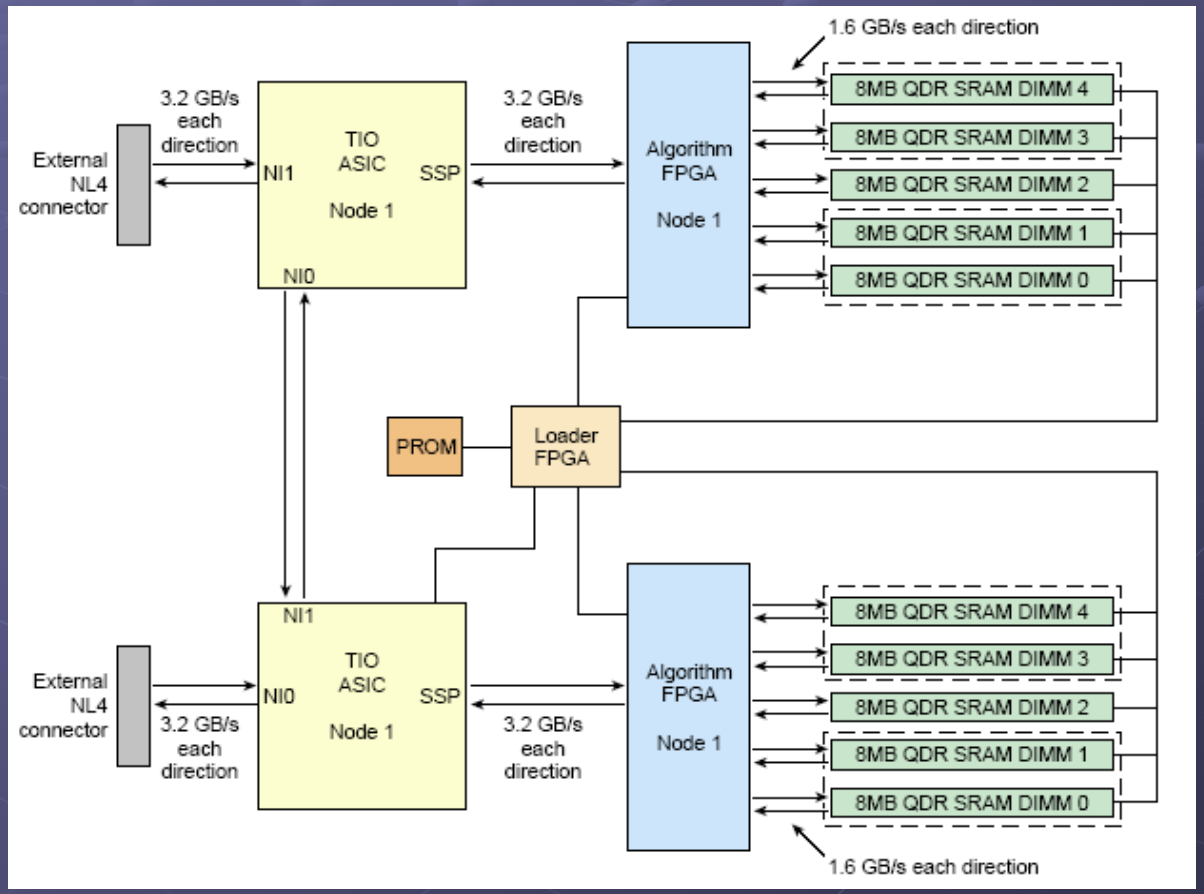
Loop profiling tool for HPC code inspection as a method of efficient FPGA based acceleration

Marcin Pietroń, Paweł Russek, Kazimierz Wiatr

Hardware platform (**SGI Altix 4700**)



Loop profiling on Gaussian

- analysis and instrumentation of f77 code
- two types of loops:

```
      DO 100 I=1,100                    DO  WHILE (…)
       .                                 .
       .                                 .
100   END                               END DO
```

- loop profiler is a step for further analysis of code (e.g. prepare data for DFG generating)

Loop profiling on Gaussian

- loop profiler extract following data:

  - time of execution of each loop
  - number of enter of each loop
  - number of iterations
  - loop dependencies (loop graph)
  - data dependencies in loops (for loop pipelining and paralleling)

Loop profiling -> MitrionC

- MitrionC – HLL language for FPGA in HPC (dedicated for SGI RASC platform)
- loop profiler extracts loops that can be speedup in MitrionC language
- speedup by using *foreach* and *while* MitrionC loops