Reconfigurable platforms

RASC platform

FPGAs: 2 x Virtex 4 LX200
Memory: 80MB QDR SRAM
Interface: Dual NUMAlink™ 4 ports

Node available on PANDA supercomputer

PICCO platform

Picco Spartan 6

FPGAs: 6 x Xilinx Spartan 6 LX150
Memory: 256 MB DDR3

Picco Virtex 6

FPGAs: 2 x Xilinx Virtex 6 LX240
Memory: 2GB DDR3, 8MB QDRII

Nodes available on ZEUS supercomputer

Cyfronet computing offer is extended beyond traditional computing solutions. In an addition to the SMP and cluster solutions, the Center also provide a reconfigurable computing platforms for conducting calculations those are performed by dedicated architecture. Thus, application execution can be accelereted allowing fot even order of magnitude speedup for some application cases.

Reconfigurable systems of this type are widely used in scientific and technical HPRC (High Performance Reconfigurable Computing) calculations. To date, applications of reconfigurable systems succesfully proved effectivness in such HPC areas as: genomics, data mining (called data mining), traffic simulation, financial applications, etc.

Reconfigurable logic structure is described in a 'C' like programming language (Impulse-C) or alternatively in hardware description languages.

HPRC computations

Increasing resources offered by FPGAs have enabled their efficient utilization for large-scale computing. Also, the development of tools for the FPGAs design contributes to the dissemination of FPGAs in HPC world. Today, the creation of the dedicated processor in FPGA more and more resembles software programming rather than the hardware design process.
Conventional processors are very efficient in performing of common operations. For such operations the use of FPGAs is not adequate. There are many algorithms however that do not fit into the structure of general purpose processors, for example, in terms of the type of data representation and used operations. A given example can be a 1-bit representation and Boolean operations. Such applications, which also provide the possibility of parallel computation, are ideal candidates for acceleration using reconfigurable systems. Algorithms weel suited for FPGA are data processing algorithms which expose locality and do not require high data transfer to and from the processor.

For more information:

RASC platform - RASC Introduction
PICCO platform - Product Overview

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